



Sardar Vallabhbhai National Institute of Technology, Surat - 395007,  
Gujarat

Department of Electrical Engineering

Department of Electrical Engineering  
Room No. 17/S.V.N.I.T., Surat-7  
આવક નં./INWARD No.:  
જારી નં./OUTWARD No.: 1892  
Date: 04.12.2023 4/12/23

## Notice

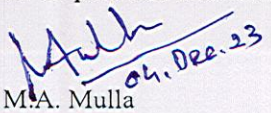
With reference to the advertisement (no. DoEE/ 1716 Date: 31/10/2023) for the post of Junior Research Fellow (JRF)-(01) on a purely contract basis for the research project “*Design and Development of Smart BMS with Cell Surface Temperature Estimation*” funded by the Science and Engineering Research Board (SERB), DST, Government of India the offline interview of eligible candidates will be conducted at SVNIT campus, Department of Electrical Engineering, Room no: EN-17 (Seminar Hall) on 21-Dec-2023.

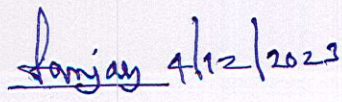
### List of Eligible Candidates

Sr. No	Name of the Candidate	Offline Interview at SVNIT Surat
1.	Aabid Chandbasha Mulla	9.30-10.00 AM
2.	Bagle Hiren Jagdishbhai	10.00-10.30 AM
3.	Bhavin Pravinbhai Ornawala	10.30-11:00 AM
4.	Joshi Priyanka	11:00-11.30 AM
5.	Keyur Patel	11.30 AM-12:00 Noon
6.	Krutika Solanki	12:00 Noon -12:30PM
7.	Mohan Das	12:30 PM - 01:00 PM
8.	Swati Gupta	01:30 PM - 02:00 PM

#### Note:

- (1) Please bring all original certificates, such as mark sheets and degree certificates
- (2) All candidates are requested to report to the undersigned by **9:00 AM on 21-Dec-2023**
- (3) Bring one set of filled JRF application form and Xerox copies of eligibility/ qualification documents.
- (4) No TA/DA will be paid for attending the interview.

  
Dr. M.A. Mulla  
Principal Investigator, DoEE  
Email: [mam@eed.svnit.ac.in](mailto:mam@eed.svnit.ac.in)

  
Dr. Sanjay Tolani  
Co-Principal Investigator, DoEE

  
Prof. Ashish K Panchal  
Chairman of DRCC and HOD, DoEE